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Selected US specifications from IPC sub-class
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(54) Digital signal processing system

(57) A digital signal processing system for use as a digital service unit within a communication switching system, comprised of a plurality of digital signal processing (DSP) modules for connection via a dedicated programmable digital switch forming part of a circuit switch matrix 3, to one or more input/output ports such as line circuits 5A, trunk circuits 5B, etc., under control of a main system controller 1, such as a microprocessor. Applications programs for implementing predetermined service features, are downloaded from the main controller via the circuit switch matrix and digital switch, to one or more of the digital signal processing modules for storage within internal memories thereof. The main controller dynamically allocates circuit switch and message channels of the programmable digital switch in accordance with the signal bandwidth and computation power required to implement the predetermined service features. Thus, an extremely high signal bandwidth efficiency is obtained for performing various service features such as tone generation and detection, DTMF tone detection, digital conferencing, speech synthesis, etc., utilizing simple, inexpensive, time-shared modules.

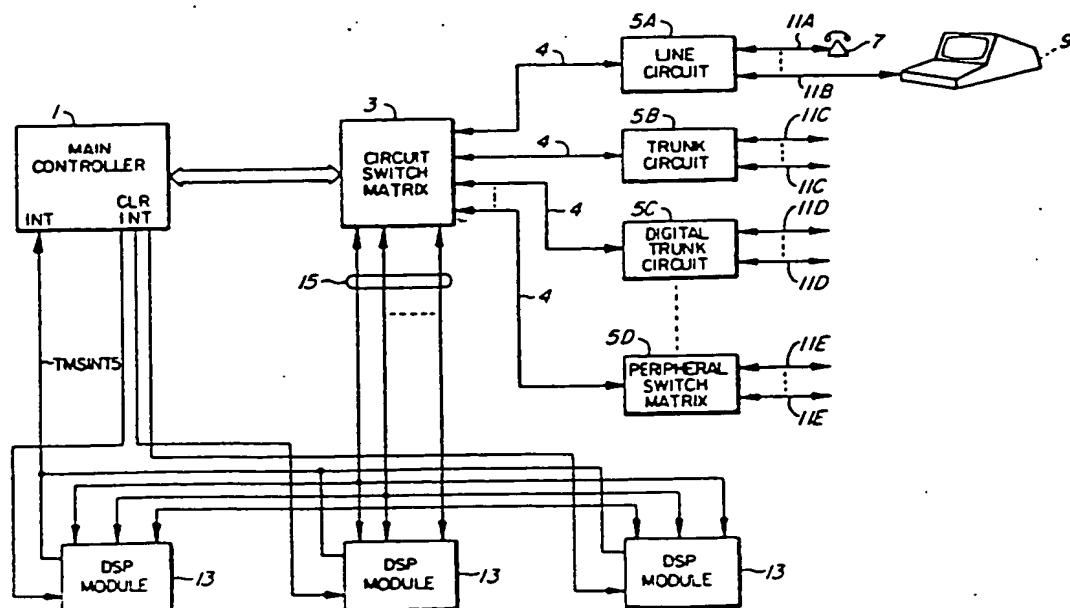


FIG. 1

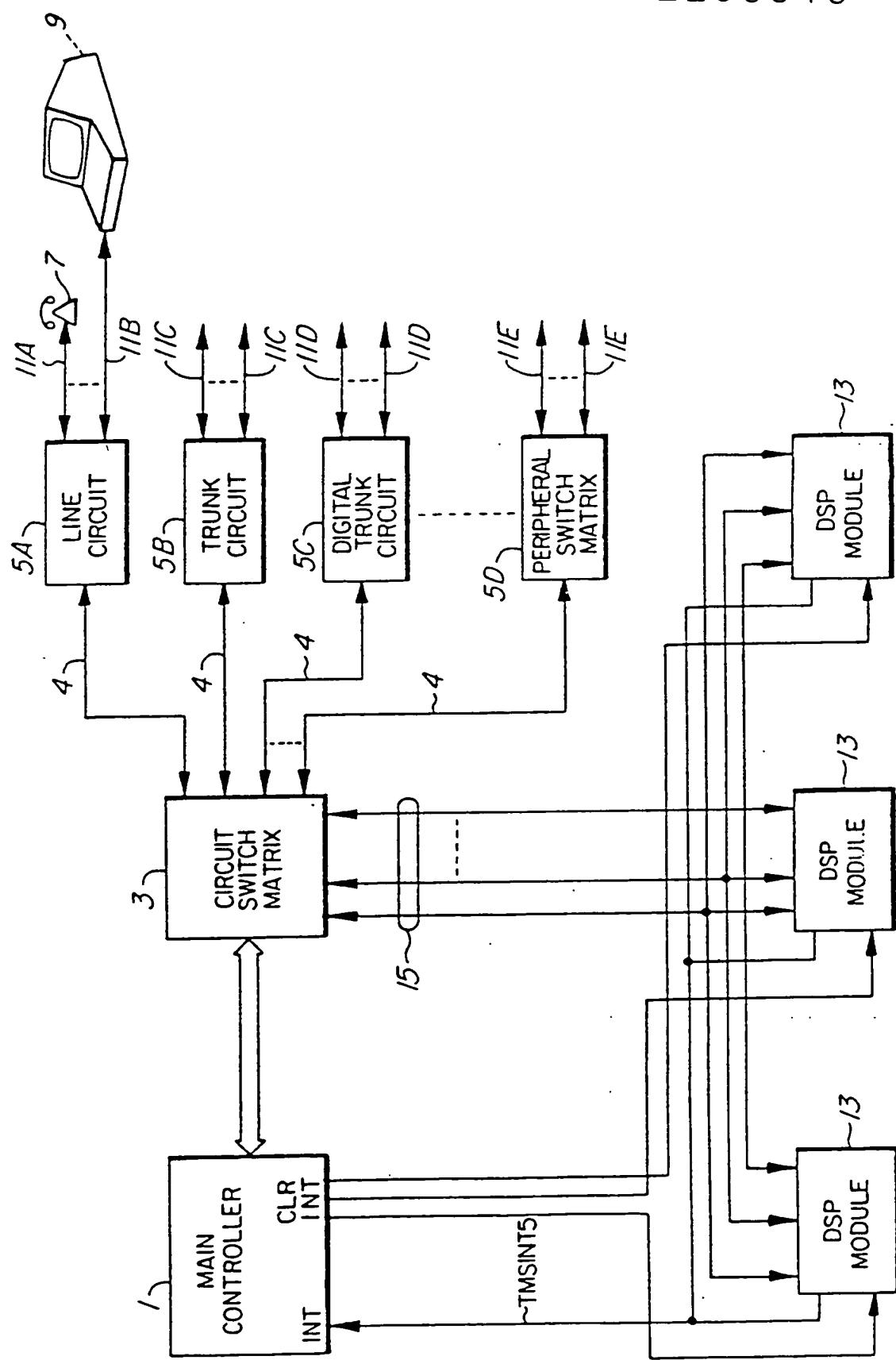


FIG. 1

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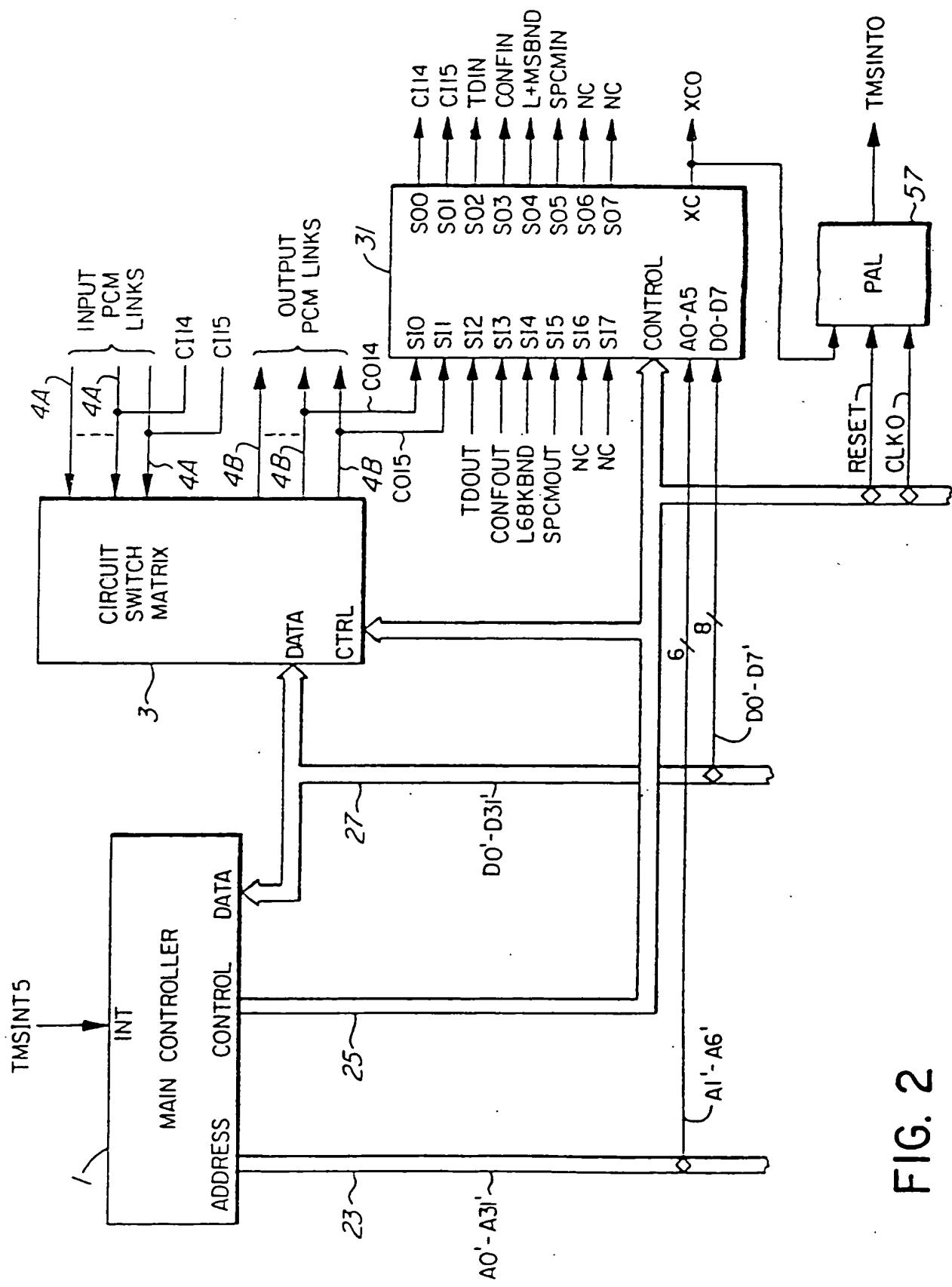


FIG. 2

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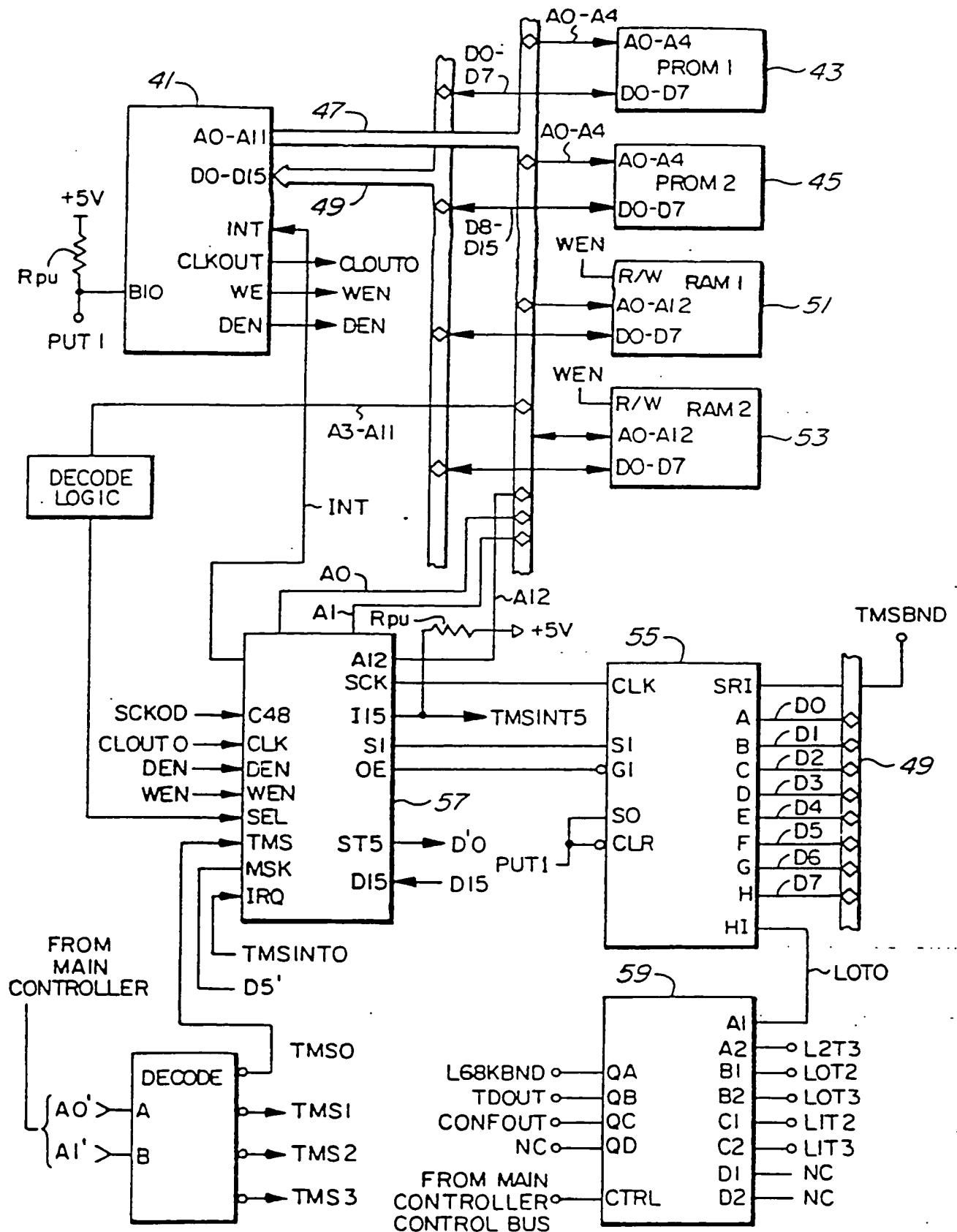


FIG. 3

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01 DIGITAL SIGNAL PROCESSING SYSTEM

02 This invention relates to telephone
03 systems in general, and more particularly to a digital
04 signal processing system for use as a digital service
05 unit within a communications switching system.

06 Digital service units (DSUs) are used in
07 modern day communications systems such as PABXs, to
08 provide such features as tone generation, tone
09 detection, and conferencing.

10 Prior art DSUs typically incorporated a
11 plurality of circuits dedicated to provision of
12 respective ones of the aforementioned features. Tone
13 detection circuitry, tone generation circuitry and
14 call conferencing circuits were typically all disposed
15 on respective printed circuit boards comprising
16 discrete components, and were rack mounted in a
17 cabinet, such as a PABX equipment cabinet.

18 The prior art circuitry typically occupied
19 considerable circuit board area, and was characterized
20 by high cost, circuit complexity and little or no
21 capacity for expansion. In addition, many of the
22 prior art DSUs employed analog circuitry which was
23 prone to distortion and low accuracy performance due
24 to temperature drift, etc.

25 In an embodiment to be described, a
26 digital signal processing system is provided for
27 implementing features such as digital tone generation,
28 digital conferencing, DTMF tone detection, progress
29 tone detection, and speech synthesis, as well as
30 others. According to a preferred embodiment, the
31 features are implemented digitally via a dedicated
32 digital signal processing (DSP) module comprised of a
33 digital signal processing chip, one or more random
34 access memories and a programmable logic array (ULA)
35 embodying DSP support logic circuitry for interfacing
36 the DSP chip. One or more of such DSP modules are
37 connected via time divided digital signal links to a
38 dedicated digital crosspoint (DX) switch.

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02 A central processor or main controller supervises
03 interaction between the DX switch and the DSP modules.

04 Unlike prior art DSUs which typically
05 employed dedicated paths for circuit switching and
06 messaging, according to the present invention circuit
07 switching and message communication are combined on
08 one or more shared DX links wherein the portions of
09 the link bandwidth dedicated to messaging and circuit
10 switching are controlled by the main controller and
11 are dependent on which of the service features is
12 being implemented. For instance, in the event the
13 desired service feature requires a large amount of
14 signal processing computation time to implement but
15 has low input/output signal traffic, then relatively
16 few circuit switch channels are allocated. However, if
17 the feature requires little computation power but wide
18 input/output bandwidth, a large number of circuit
19 switch channels are allocated.

20 The DX switch is addressed by the main
21 controller via parallel address and data ports in
22 order to dynamically allocate channels for
23 establishing message and circuit switch paths to each
24 DSP module, and an interrupt handshaking scheme is
25 implemented between the DX switch and DSP modules for
26 controlling transmission of message information
27 packets therebetween. The packets can be either
28 applications programs for downloading to one or more
29 of the DSP modules, or interrupt and control signals
30 for supervising the timing and execution of the
31 programs.

32 An important characteristic of the preferred
33 embodiment is that a digital DX switch is utilized in
34 connection with the one or more DSP modules for
35 providing combined message and circuit switching via
36 dynamically allocated message and circuit switch
37 channels. Thus, a plurality of service features are
38 accommodated with a minimum of circuit complexity and

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02 cost.

03 A better understanding of the present
04 invention will be obtained with reference to the
05 detailed description below in conjunction with the
06 following drawings, in which:

07 Figure 1 is a block diagram of a digital
08 signal processing system in accordance with the
09 present invention,

10 Figure 2 is a block schematic diagram of a
11 main controller, circuit switch matrix and dedicated
12 digital DX switch according to the preferred
13 embodiment of the present invention, and

14 Figure 3 is a block schematic diagram of a
15 digital signal processing module according to the
16 preferred embodiment.

17 With reference to Figure 1, a main
18 controller 1 is shown connected to a circuit switch
19 matrix 3 having a plurality of input/output ports such
20 as line and trunk circuits 5A-5C and a peripheral
21 switch matrix 5D connected thereto. A subscriber set
22 7 and a data terminal 9 are shown connected to a
23 representative one of the line circuits 5A via
24 bidirectional PCM links 11A and 11B. PCM links 11A
25 can be replaced by well known balanced bidirectional
26 telephone lines in the event that the subscriber set 7
27 is a standard 500 type telephone set. In this case,
28 the line circuit 5A typically also includes a
29 digital-to-analog and analog-to-digital converter for
30 translating between analog signals on the telephone
31 line and PCM encoded signals transmitted to and from
32 the circuit switch matrix 3.

33 Trunk lines may be connected to the trunk
34 circuit 5B extending from a telephone central office
35 via the lines 11C, and digital trunks (such as the
36 industry standard T1 trunk) may be connected to the
37 digital trunk circuit 5C. The peripheral switch
38 matrix 5D may be connected via links 11E to additional

02 expansion line and trunk circuits in a well known
03 manner.

04 A plurality of DSP modules 13 are
05 connected via dedicated PCM links 15 to the circuit
06 switch matrix 3. Each of the DSP modules 13 has a
07 control output thereof for generating an interrupt
08 signal TMSINT 5 for interrupting the main controller
09 1. The TMSINT 5 signal output from individual ones of
10 the DSP modules 13 is a high impedance output, and
11 each signal is applied to a common interrupt line
12 forming a logic OR function. The main controller 1
13 generates respective interrupt clear signals for
14 resetting interrupts generated by the DSP modules 13.

15 In operation, the main controller 1
16 configures a predetermined switching element or DX
17 switch (discussed below with reference to Figure 2) of
18 the circuit switch matrix 3 for dynamically allocating
19 predetermined PCM channels of the shared links 15 for
20 establishing a message signal path between the circuit
21 switch matrix 3 and each DSP module 13. An interrupt
22 handshaking scheme is utilized to establish
23 communication between the main controller 1 and DSP
24 modules 13 utilizing the aforementioned interrupt
25 signals.

26 For example, a predetermined DSP module 13
27 can generate a TMSINT 5 interrupt control signal for
28 application to the INT input of the main controller
29 1. In response, the main controller generates a
30 message signal packet for transmission along a
31 dedicated message signal channel of a predetermined
32 dedicated message signal channel of a predetermined
33 one of the PCM links 15 via circuit switch matrix 3,
34 for storage in an internal memory of the DSP module
35 13. The main controller 1 then generates an
36 appropriate clear interrupt signal via a CLRINT output
37 thereof for causing the selected DSP module 13 to
38 reset its TMSINT 5 signal output. The DSP module 13

02 then generates another TMSINT 5 interrupt signal for
03 causing the main controller 1 to transmit a second
04 message signal packet, and the procedure is repeated
05 until an entire program has been downloaded.

06 The message signal packets can be, for
07 instance, in the form of an applications program code
08 for execution by one or more of the DSP modules 13,
09 resulting in implementation of a predetermined service
10 feature.

11 Once the internal memory of the DSP module
12 has been loaded with the applications program, the
13 code is executed by the DSP module for performing one
14 of either tone plant, digital conferencing, DTMF or
15 ATD tone detection, speech synthesis, etc.

16 For example, in order to implement the
17 speech synthesis service feature, one or more encoded
18 messages are first stored on a disk (not shown), such
19 as Winchester disk connected to the main controller
20 1. The main controller 1 then transmits the encoded
21 messages to a predetermined one of the DSP modules 13
22 via allocated message channels of the PCM links 15
23 through circuit switch matrix 3. The selected DSP
24 module 13 executes the stored applications program and
25 converts the encoded messages into A-law or μ -law
26 encoded PCM signals and transmits the PCM signals via
27 further allocated channels (circuit switch channels)
28 of the PCM links 15 to one or more of the line or
29 trunk circuits 5A-5D.

30 Since the PCM channels are dynamically
31 allocated, as many or as few of the channels are
32 utilized by a predetermined DSP module 13 as required
33 for implementing the particular service feature.
34 Thus, if the service feature requires considerable
35 computation time for the applications program to be
36 executed, the channel bandwidth is low (eg. four or
37 five allocated circuit switch channels are used for
38 tone detection). However, if the DSP program requires

02 little computation time but high signal throughput, a
03 large number of circuit switch channels may be
04 allocated, (for example forty-two channels are used
05 for implementing the tone plant feature).

06 As a further example, digital conferencing
07 can be implemented according to the present invention,
08 by programming a predetermined one of the DSP modules
09 13 for receiving voice or tone signal samples from
10 predetermined ones of the line, trunk or peripheral
11 matrix circuits 5A-5D via the circuit switch matrix 3
12 and dedicated circuit switch channels of PCM links
13 15. The DSP module 13 detects the "loudest" one of
14 the signal samples (i.e. the sample having the largest
15 magnitude) and sends that sample to each of the signal
16 sources connected to the line or trunk circuits 5A-5D
17 except for the signal source from which it was
18 generated. The second loudest signal sample is then
19 transmitted to the source of the loudest signal
20 sample.

21 The tone detection feature of the present
22 invention can be implemented by a predetermined one or
23 more of the DSP modules 13 by receiving a number of
24 tone signal samples from one or more of the circuits
25 5A-5D via circuit switch matrix 3 and dedicated
26 circuit switch channels of the PCM links 15, and
27 performing thereon. A well known tone detection
28 algorithm performs a discrete Fourier transform on the
29 received tone samples and generates a message signal
30 along a further dedicated message signal channel of
31 the PCM links 15 to the main controller 1, indicative
32 of whether or not a predetermined DTMF tone is
33 present.

34 Additional features can be performed by
35 the digital signal processing system of the present
36 invention. For example, type-written messages from a
37 data terminal, such as data terminal 9, can be
38 transmitted via line circuit 5A, through circuit

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02 switch matrix 3, and along a dedicated message channel
03 of the PCM link 15 to a predetermined one of the DSP
04 modules 13. In response, the DSP module 13 can
05 implement a text-to-speech conversion algorithm or a
06 direct speech synthesis algorithm for generating
07 "canned messages" along further circuit switch
08 channels of the PCM links 15 via circuit switch matrix
09 3 to other ones of the subscriber sets 7 or terminals
10 connected to the input/output ports 5A-5D.

11 Thus, the digital signal processing system
12 as illustrated in Figure 1 provides many of the same
13 features as prior art digital service units (DSUs),
14 plus many more. However, as discussed above, prior
15 art DSUs typically require dedicated paths for circuit
16 switch signals and message signals, whereas according
17 to the present invention both functions are
18 dynamically allocated between single or multiple PCM
19 links 15, wherein the proportion of channels devoted
20 to either of message or circuit switch signalling
21 varies as the application demands.

22 An important element of the system
23 embodying the present invention is the DX switch,
24 discussed in greater detail below with reference to
25 Figure 2. The DX switch is a combined programmable
26 time and space switching circuit utilized within the
27 circuit switch matrix 3 for dynamically allocating PCM
28 channels of the links 15 to the DSP modules 13 in
29 order to support simultaneous combined message and
30 circuit switch signalling.

31 A detailed description of the DX switch
32 can be found in Canadian patent No. 1,171,946 entitled
33 TIME DIVISION SWITCHING SYSTEM, issued July 31, 1984
34 to Mitel Corporation, to which the reader is referred.

35 With reference to Figure 2, the main
36 controller 1 is shown in greater detail having an
37 address bus 23, control bus 25 and data bus 27
38 connected thereto. The main controller typically

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02 includes a microprocessor, such as the Motorola
03 MC68020 microprocessor in conjunction with support
04 logic circuitry and one or more disk drives and RAM
05 memory circuits (not shown). According to a
06 successful prototype of the present invention, 4
07 megabytes of RAM were provided and the MC68020 was
08 utilized for controlling a communication switching
09 system with up to 300 lines, (such as the lines or
10 links denoted as 11A-11E in Figure 1).

11 According to the preferred embodiment, the
12 address bus 23 is comprised of 32 address lines
13 A0'-A31', the data bus 27 is comprised of 32 data
14 lines D0'-D31' and the control bus 25 is comprised of
15 a plurality of well known control signal carrying
16 lines, such as READ/WRITE, CHIP ENABLE, RESET, and
17 various timing and clock signals.

18 A PAL™ device 61 is connected to
19 predetermined lines of the control bus 25 designated
20 RESET, TMSG, CLKOUT 0, CLKOUT 1 and CLKOUT 2, as well
21 as to input and output ports of the circuit switch
22 matrix 3 designated XC1 and XC2, and to a DX switch 31
23 which generates the signal designated as XCO.

24 Circuit switch matrix 3 is connected to
25 the main controller 1 via DATA and CTRL ports thereof,
26 as well as preferably an address port (not shown).
27 Input and output links 4A and 4B carry unidirectional
28 circuit and message switch signals between various
29 external input/output ports such as line circuit 5A,
30 trunk circuit 5B, etc., as illustrated in Figure 1.

31 The dedicated DX switch 31 is provided for
32 dynamically allocating message and circuit switch
33 channels of PCM links 15 (Figure 1), and is shown for
34 the purpose of explanation as being separate from the
35 circuit switch matrix 3, but is actually incorporated
36 as an element thereof.

37 DX switch 31 is preferably a programmable
38 digital combined time and space division switch such

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02 as the Mitel Model MT8980 digital time/space
03 crosspoint switch, as described in the aforementioned
04 Canadian patent 1,171,946 of Mitel Corporation.

05 The patented DX switch 31 has a number of
06 useful features, including the ability to receive
07 message signals on the data inputs D0-D7 thereof for
08 conversion to serial format and transmission along
09 allocated message channels of the PCM links connected
10 to serial output ports S00-S07. Similarly, serial
11 message signals can be received on input ports SI0-SI7
12 and transmitted via parallel data ports D0-D7 to the
13 main controller 1 along the data bus 27.

14 A predetermined pair (CI14 and CI15) of
15 the input PCM links 4A are also connected to serial
16 PCM output terminals S00, and S01 of the DX switch 31,
17 and a predetermined pair (CO14 and CO15) of the output
18 PCM links 4B from matrix 3 are connected to serial
19 input terminals SI0 and SI1 of the DX switch 31.

20 Serial inputs SI2 to SI4 and outputs
21 S02-S04 are connected to various ones of the DSP
22 modules 13 (Figure 1). For example, the SI2 input and
23 S02 output carry signals TDOUT and TDIN respectively,
24 and are connected to a predetermined one of modules 13
25 for performing tone detection and tone generation.
26 The SI3 input and S03 output carry signals denoted as
27 CONFOUT and CONFIN respectively and are connected to a
28 further DSP module 13 for performing digital
29 conferencing of up to nineteen PCM channels, as
30 discussed above. The SI4 input and S04 output carry
31 signals L68kBND and LTMSBND respectively, and are
32 connected to a further DSP module 13 for implementing
33 a DTFM receiver or tone detection function, as
34 described above.

35 Input SI5 and output S05 are connected to
36 an HDLC protocoller (not shown) which is used to
37 transmit and receive HDLC framed message signals from
38 various circuit or message links, such as 11A-11E,
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02 etc. The HDLC protocoller does not form part of the
03 present invention and will not be described in further
04 detail.

05 The SI6, SI7 inputs and S06, S07 outputs
06 are shown as being not connected. However, serial
07 ports SI6 and S06 can be connected, for example, to a
08 maintenance panel for servicing or performing
09 diagnostics, while the SI7 and S07 ports can be
10 connected to a mate processor for effecting a
11 redundant back-up system.

12 The PAL™ device 61 synchronizes a timing
13 interrupt signal received from the XC terminal of DX
14 switch 31, to the synchronous clock associated with
15 each of the DSP modules 13. This interrupt is used by
16 applications software running in the DSP modules 13 to
17 define event windows in which message or circuit
18 switch data may be transmitted between the DSP modules
19 13 and DX switch 31.

20 While each of the DSP modules 13 is
21 preferably of similar design, the applications
22 programs which are executed serve to characterize the
23 individual service features which are implemented
24 thereby.

25 A detailed description of the operation of
26 one of the DSP modules 13 as a DTMF tone detector,
27 will now be described in detail, by way of example.

28 With reference to Figure 3, a
29 representative one of the DSP modules 13 is shown in
30 greater detail. A digital signal processing circuit
31 41, such as the TMS 320 model digital signal processor
32 manufactured by Texas Instruments, is connected to
33 address ports A0-A4 of a pair of programmable ROM
34 circuits 43 and 45 via address bus 47, and data ports
35 D0-D7 thereof via a data bus 49. The address and data
36 buses are connected to A0-A11 and D0-D15 terminals
37 respectively, of DSP circuit 41. The PROM circuits 43
38 and 45 contain a bootstrap program for initializing

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02 DSP circuit 41 to interrupt the main controller 1
03 (Figure 2) in order to start receiving message packets
04 containing the applications program code for storage
05 in a pair of random access memories (RAMs) 51 and 53,
06 as discussed above with reference to Figure 1.

07 RAM circuits 51 and 53 have address inputs
08 A0-A12 thereof connected to the address bus 47, and
09 D0-D7 data terminals thereof connected to the data bus
10 49. READ/WRITE control terminals of the RAM circuits
11 51 and 53 are connected to a write enable output WE of
12 DSP circuit 41 for receiving a write enable signal
13 (WEN) therefrom.

14 A serial-to-parallel converter 55 receives
15 the TMSBND signal from serial output S04 of the DX
16 switch 31 (Figure 2) on a serial input SRI thereof,
17 and converts it to an eight bit parallel format for
18 transmission via parallel A-H outputs to the D0-D7
19 data lines of data bus 49 connected to DSP circuit 41.

20 The serial-to-parallel converter 55 also
21 received parallel format signals from data bus 49 and
22 generates a serial PCM signal designated LOTO from a
23 serial output HI thereof, for application to the A1
24 input of a multiplexer 59, which in turn passes the
25 signal (designated as L68KBND) via the QA output
26 thereof to the SI4 serial input terminal of DX switch
27 31 (Figure 2), under control of the main controller 1.

28 Additional serial output signals L2TS,
29 LOT3, LIT2 and LIT3 are applied to the A2, B1, B2, C1
30 and C2 inputs of multiplexer 59 respectively, from
31 additional DSP modules 13 (not shown in detail) for
32 implementing the aforementioned digital conferencing,
33 tone plant, ATD tone detection service features, etc.
34 These additional signals are multiplexed and appear on
35 the QA, QB and QC outputs as L68KBND, TDOUT and
36 CONFOUT, respectively.

37 A plurality of logic support circuits are
38 embodied within a programmable array designated as

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02 PAL™ device 57, for controlling timing, enabling, and
03 data transfer between the main controller 1, DSP
04 circuit 41 and bidirectional serial-to-parallel
05 converter 55.

06 In operation, during initialization, the
07 main controller 1 establishes or allocates
08 predetermined message signal paths through DX switch
09 31 for reception by DSP circuit 41 via converter 55.
10 The main controller 1 then resets the DSP circuit 41
11 for causing execution of the bootstrap program stored
12 in PROM circuits 43 and 45 in a well known manner.
13 The bootstrap program causes DSP circuit 41 to
14 generate an interrupt signal to the main controller 1
15 for initializing transfer of message signals between
16 the main controller 1 and DSP circuit 41, as discussed
17 above.

18 In particular, the DSP circuit 41 causes a
19 TMSINT 5 tristate interrupt signal to be generated by
20 PAL™ device 57 in response to a logic high signal
21 appearing on the ST5 output thereof and a logic low
22 signal being applied to the MSK input thereof. The
23 signal appearing on the MSK input is received from the
24 D5' data line of the data bus 27 connected to main
25 controller 1 (Figure 2). A logic high signal output
26 from the ST5 output of PAL™ device 57 is generated
27 in response to the occurrence of logic high signals
28 being applied to the SEL, DEN and AO inputs and logic
29 low signals being applied to the A1 and TMS inputs
30 thereof. The logical operation of PAL™ device 57 is
31 shown below with reference to the following truth
32 table.

TABLE 1

AO A1 /MSK /C48 CLK /DEN /WEN SEL /TMS GND
/IRQ /OE /ST5 /A12 SI /SCK /INT /IL5 /D15 VCC

IFD (SEL * DEN * /AO * /A1) D15 = /ST5 ; read with port 4

IF (VCC) INT = /CLK * IRQ ; interrupt to TMS
+ CLK * INT
+ INT * IRQ

IF (VCC) SCK = C48 ; Port 4 Write
+ SEL * WEN * /A1 * /AO

IF (VCC) /SI = /SCK ; the one load condition
+ /SEL ; all ram acceses
+ A1 ; port 6,7 writes
+ AO ; port 5,7 writes
+ /WEN * /SI ; all reads

IF (VCC) A12 = SEL * DEN * A1 * /AO ; page bit
+ A12 * /SEL ; hold it
+ A12 * /DEN
+ A12 * /A1
+ A12 * /AO ; hazard term for latching

IF (VCC) ST5 = SEL * DEN * /A1 * AO * /TMS ; interrupt bit
+ ST5 * /TMS

IF (ST5 * /MSK) IL5 = ST5 * /MSK ; Tristate int

IF (VCC) OE = SEL * DEN * /A1 * /AO ; Port 4 read

02 As soon as the main controller 1 receives
03 the interrupt signal TMSINT 5, it writes a byte of
04 message information for transmission via data bus 27
05 to the D0-D7 input of DX switch 31. DX switch 31
06 converts the parallel format message signal into
07 serial format for transmission via the aforementioned
08 serial output S04 (which comprises one of the
09 aforementioned PCM links 15 discussed with reference
10 to Figure 1). The serial format message signal is
11 received by serial-to-parallel converter 55 on the SRI
12 input thereof. The converter 55 reconverts the serial
13 message signal to parallel format for application to
14 data bus 49 and storage in RAM circuits 51 and 53
15 under control of DSP circuit 41. Each time an
16 interrupt is generated by DSP circuit 41, an internal
17 counter of DSP circuit 41 is incremented, and the
18 received message byte from main controller 1 is stored
19 in RAM circuits 51 and 53, which according to the
20 successful prototype were capable of storing up to a
21 maximum of 16k bytes.

22 Once the main controller 1 has written a
23 new byte into the allocated message channel within DX
24 switch 31, it generates a further signal via the
25 control bus 25 for application to the PAL[™] device 57
26 which in response generates a "clear interrupt" signal
27 which clears the original interrupt signal TMSINT 5
28 and an internal interrupt status bit (ST5) thereof,
29 which is periodically read by DSP circuit 41 from an
30 input/output port thereof via the D15 data line.

31 As discussed above, the DSP circuit 41
32 according to the successful prototype, was a TMS 320
33 digital signal processing chip. The TMS 320 chip
34 latches interrupts internally, such that a low signal
35 appearing on the INT input thereof for one bit period
36 is typically sufficient for causing an interrupt to
37 occur.

38 The logical operation of PAL[™] device 61

with respect to the aforementioned representative one of the DSP modules 13, is shown below with reference to the following truth table 2.

TABLE 2

```
/RESET /XCO CLKO GND
/SO /TMSINTO VCC
;
; TMS interrupt synchronization
;
IF (/RESET) SO      = /CLKO* XCO          ; first stage
    +  CLKO* SO
    +  XCO * SO
;
IF (/RESET) TMSINTO =  CLKO* SO          ; second stage
    + /CLKO* TMSINTO
    +  SO  * TMSINTO
; latches on rising edge
; latches on falling edge
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02 In actual fact PAL™ device 61 includes
03 many more input and output terminals for connection to
04 various additional DSP modules 13, (not shown) for
05 controlling timing and synchronization thereof.

06 Thus, applications programs, such as
07 service feature programs, are downloaded from the main
08 controller 1 for storage in RAMs 51 and 53 thereby to
09 be executed by DSP circuit 41 for implementing service
10 features such as the aforementioned DTMF receiver
11 function.

12 Having downloaded the program, the main
13 controller 1 resets and initializes DSP circuit 41 by
14 generating predetermined control signals to PAL™
15 device 57 for causing generation and application of an
16 interrupt signal (INT) to the interrupt input of DSP
17 circuit 41. This starts execution of the code from
18 RAM circuits 51 and 53. The DX switch 31 is then
19 configured to allocate predetermined message and
20 circuit switch channels as required by the specific
21 service feature being implemented.

22 During execution of the service feature
23 applications program, the DX switch 31 generates a
24 timing interrupt to DSP circuit 41 via the XC output
25 thereof for controlling timing of execution of the
26 program. In particular, an interrupt signal XCO is
27 transmitted on a per time slot basis from DX switch
28 31, and depending on the particular program being
29 executed by DSP circuit 41, the XCO signal can assume
30 various formats. For example, three interrupts
31 followed by a gap may indicate a message signal
32 transfer, and six continuous interrupts may indicate a
33 data transfer. The spacing which is used for message
34 and data switching typically varies in relation to the
35 particular program being implemented.

36 For example, when implementing the tone
37 plant service feature, only one interrupt from the DX
38 switch 31 is required to identify where the first PCM

02 channel, (i.e., channel 0) will be located in the next
03 PCM frame on the predetermined link 15. However, for
04 the DTMF tone detector program, one message interrupt
05 causes transmission of a message packet to the main
06 controller 1 for indicating the occurrence or
07 non-occurrence of a predetermined tone.

08 The XCO signal from DX switch 31 is
09 synchronized and presented to the interrupt input INT
10 of DSP circuit 41 via PAL[™] devices 61 and 57. In
11 particular, the XCO signal from DX switch 31 is
12 applied to an input of PAL[™] device 61 of the main
13 controller 1 which in response generates the TMSINTO
14 interrupt discussed above which is applied to the IRQ
15 input of PAL[™] circuit 57. In response, and in
16 accordance with the logic conditions discussed above
17 in connection with Table 1, PAL[™] device 57 generates
18 an INT interrupt signal for application to the INT
19 input of DSP circuit 41.

20 The XCO interrupt received from the DX
21 switch 31 also synchronizes the DSP circuit 41 with
22 the timing on the PCM signal links 15 (Figure 1) in
23 order that it may read or write data to or from the
24 serial-to-parallel converter 55 during predetermined
25 channel time slots.

26 PCM signals are received by circuit switch
27 matrix 3 on input PCM links 4A, and are switched
28 therethrough for appearance on one or both of output
29 PCM lines CO14 and CO15 which are applied to the SIO
30 and SII serial input terminals of DX circuit 31, as
31 discussed above. In response, DX circuit 31 switches
32 the incoming PCM signal data in one or both of time
33 and space, to appear on the SO4 serial output terminal
34 thereof in one or more predefined dynamically
35 allocated channels.

36 The input PCM signals are received on the
37 SRI input of converter 55 as discussed above, and
38 presented to the data bus 49 for manipulation or

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02 processing via DSP circuit 41 to detect whether one or
03 more DTMF tones are present, according to a
04 predetermined algorithm implemented as a result of DSP
05 circuit 41 executing a predetermined applications
06 program.

07 DSP circuit 41 reads and writes data on
08 data bus 49 for application to the converter 55 at
09 specific times in accordance with the timing control
10 provided by PAL[™] circuit 57. Thus, a message signal
11 indicative of the presence or absence of DTMF tones is
12 output in serial form via the HI output of converter
13 55 and transmitted to multiplexer 59 for appearance on
14 the QA output thereof as the L68kBND signal, and also
15 applied to the SI4 input of DX switch 31. The DX
16 switch 31 passes the signal to circuit switch matrix
17 3, and from there to the main controller 1 or to the
18 various input/output ports. The main controller 1
19 then takes appropriate action within the communication
20 system such as, for example, configuring the circuit
21 switch matrix 3 to interconnect two or more of the
22 input/output ports to establish a communication link
23 therebetween.

24 It will be understood that while the
25 operation of one of the DSP modules 13 has been
26 described in relation to implementation of a DTMF tone
27 detection service feature, other features (such as
28 tone plant, digital conferencing, speech synthesis,
29 etc.,) can be performed by the DSP modules 13 in
30 response to execution of appropriate applications
31 programs downloaded from the main controller 1, as
32 discussed above.

33 According to the successful prototype,
34 each one of the PCM links 15 (Figure 1) supports
35 thirty-two channels of PCM or message signal
36 communication per link, of which any given one of the
37 DSP modules 13 can utilize up to sixteen channels
38 depending on the signal bandwidth required. For

02 example, a first DSP module 13 may use even channels
03 while a second DSP module may use the odd channels.

04 As discussed, allocation of the channels
05 can be either circuit switch based or message based.
06 If the allocation is circuit switch based, the
07 channels can be used to convey audio information
08 between the input/output ports and the DSP modules 13,
09 and message information between the main controller 1
10 and DSP modules 13, for implementing tone detection,
11 conferencing, DTMF detection, tone generation, speech
12 synthesis, etc.

13 According to the successful prototype, a
14 system has been implemented utilizing a first single
15 link DSP module 13, illustrated in Figure 3, for
16 implementing DTMF tone detection; a second dual link
17 DSP module 13 for implementing digital tone
18 conferencing, and a third triple link DSP module 13
19 for performing tone generation and tone detection via
20 a two-channel DFT algorithm.

21 However, according to an alternative
22 embodiment, it is proposed that a plurality of
23 universal DSP modules 13 each having four links could
24 be implemented, wherein all of the support logic
25 connected to the DSP circuit 41, such as the PROMs 43
26 and 45, PAL[™] device 57, the serial-to-parallel
27 converter 55, etc., would be incorporated within a
28 single gate array. Each DSP module 13 would consist
29 of four chips (i.e., DSP circuit 41, RAM circuits 51
30 and 53, and the gate array) all surface mounted on a
31 small multi-layer circuit board. The modules would
32 then be easily interchangeable, resulting in flexible
33 system expansion and ease of installation, etc. Also,
34 since the service features are implemented in
35 software, maintenance and revision can be facilitated
36 by simply providing the system with upgraded
37 applications programs.

38 According to the proposed alternative

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02 embodiment, the XCO signal received from the DX
03 circuit 31, would convey more information than merely
04 interrupt signals. In particular, it is contemplated
05 that the XC link will effectively support a thirty-two
06 channel message communication path providing interrupt
07 control, link output enable, and general device
08 control for the DSP circuit 41.

09 Individual ones of the four circuit switch
10 links 15 connected to a particular one of the modules
11 13, would be programmed on a per channel basis via the
12 XC link, to be active. Thus, only the required number
13 of channels would be allocated to an individual DSP
14 module 13, to perform execution of a predetermined
15 applications program. The interface to each of the
16 PCM links 15 would be effected via a single buffer
17 shift register, such as the serial-to-parallel
18 converter 55 described above with reference to Figure
19 3.

20 Each of the thirty-two XC message channel
21 bytes would be comprised of four least significant
22 bits which indicate which of the four possible links
23 is to be enabled during the following time slot or
24 channel, as well as four most significant bits for
25 conveying command information such as channel byte
26 control, resetting, running and reading of the DSP
27 circuit 41 in either of the PROM or RAM modes, as well
28 as controlling enabling of interrupts, masking of
29 interrupts, etc.

30 Thus for example, if the most significant
31 bit is a zero, the next three bits would indicate
32 where the interrupt occurs from the DX circuit 31 to
33 the DSP module 13 in terms of bit position in the
34 following channel.

35 Alternatively, if the most significant bit
36 is a logic 1, then the next three significant bits
37 would designate one of either an idle command (no
38 operation), or seven other commands for doing

02 different instructions, such as reading the PROM or
03 RAM circuits, etc., as discussed above.

04 Thus, the service feature programs
05 executed by the DSP circuits 41 would utilize
06 dynamically allocated channels (seven channels, nine
07 channels, or three channels, etc.,) depending on the
08 bandwidth requirements of a particular application as
09 opposed to the embodiment described with reference to
10 Figures 2 and 3 wherein sixteen channels are
11 automatically allocated to each of the DSP modules
12 13. The alternative embodiment is expected to result
13 in higher efficiency of utilization of individual ones
14 of the DX links 15, and facilitate allocation of
15 functions to a plurality or "pool" of DSP modules 13.

16 A person understanding the present
17 invention may conceive of other embodiments or
18 variations thereof.

19 For instance, the DSP modules 13 may be
20 utilized to process data signals from input/output
21 ports connected to data sources. For example, the
22 circuit switch matrix 3 can be connected to receive
23 and transmit data signals to and from one or more HDLC
24 protocollers, as discussed above. The data signals
25 can then be coded, reformatted, encrypted, etc., via
26 the one or more DSP modules 13 executing predetermined
27 applications programs.

28 All such embodiments or variations are
29 considered to be within the sphere and scope of the
30 present invention as defined by the claims appended
31 hereto.

CLAIMS

1. A digital signal processing system for use in a communication system connected to a plurality of input/output ports, comprised of:

(a) main controller means for transmitting and receiving message signals,

(b) digital signal processing means for implementing one or more service features characterized by one or both of transmission and reception of PCM and message signals, and

(c) digital switching means connected to said main controller means, digital signal processing means, and input/output ports, for bidirectionally translating PCM and message signals therebetween, via one or more time divided communication links under control of said main controller means, and

(d) means for dynamically allocating predetermined channels of said one or more time divided communication links for PCM and message signal translation, wherein the proportion of channels allotted to PCM and message signal translation is dependent on which of said one or more service features is being implemented, thereby maintaining high signal bandwidth efficiency of said PCM and message signal translation.

2. A digital signal processing system as defined in claim 1, wherein said digital switching means is comprised of a combination space and time division switching matrix.

3. A digital signal processing system as defined in claim 2, wherein said digital signal processing means is comprised of one or more memory circuits for storing a predetermined service feature

applications program, and a programmable digital signal processor for executing said program and implementing a predetermined one of said service features in response thereto.

4. A digital signal processing system as defined in claim 3, wherein said digital signal processing means further includes one or more bidirectional serial-to-parallel converters for interfacing a parallel port of said digital signal processor with one or more serial links of said time division switching matrix.

5. A digital signal processing system as defined in claim 4, wherein said digital signal processing means further includes one or more read only memory circuits for storing a bootstrap program for initializing said digital signal processor.

6. A digital signal processing system as defined in claim 3, 4 or 5, wherein said serial-to-parallel converters and read only memory circuits are embodied in a single chip gate array.

7. A digital signal processing system as defined in claim 1, 2 or 3, including means for establishing an interrupt channel between said main controller means and digital signal processing means for controlling bidirectional communication of message signals therebetween.

8. A digital signal processing system as defined in claim 1, 2 or 3, further including means for establishing an interrupt channel between said digital switching means and said digital signal processing means for controlling bidirectional communication of PCM signals therebetween.

9. A digital signal processing system as defined in claim 1, 2 or 3, wherein implementation of a predetermined one of said service features is characterized by said main controller means generating a message signal designating a predetermined tone frequency for transmission on a predetermined one of said allocated channels, and digital signal processing means receiving said message signal, and in response generating a PCM tone signal at said predetermined frequency for transmission to one or more of said input/output ports on further predetermined ones of said allocated channels.

10. A digital signal processing system as defined in claim 1, 2 or 3, wherein implementation of a predetermined at least one of said service features is characterized by said digital signal processing means receiving PCM signals from predetermined ones of said input/output ports on predetermined ones of said allocated channels, detecting the relative magnitudes of respective ones of said PCM signals, and transmitting the PCM signal of second largest magnitude to the port from which the PCM signal of largest magnitude is received on a further one of said allocated channels, and transmitting the PCM signal of largest magnitude to all other ones of said ports on additional ones of said allocated channels, whereby a digital conference call is established between said predetermined ports.

11. A digital signal processing system as defined in claim 1, 2 or 3, wherein implementation of a predetermined one of said service features is characterized by said digital signal processing means receiving PCM signals from a predetermined one or more of said input/output ports along predetermined ones of said allocated channels, detecting the presence of one or more DTMF tone signals therein, and generating

message signals representative of said detected DTMF tone signals, for transmission to said main controller means on further predetermined ones of said allocated channels.

12. A digital signal processing system as defined in claim 1, 2 or 3, wherein implementation of a predetermined one of said service features is characterized by said digital signal processing means receiving PCM signals from a predetermined one or more of said external ports along predetermined ones of said allocated channels, detecting the presence of one or more ATD tone signals therein, and generating message signals representative of said detected ATD tone signals, for transmission to said main controller means on further predetermined ones of said allocated channels.

13. A digital signal processing system as defined in claim 1, 2 or 3, wherein implementation of a predetermined one of said service features is characterized by said main controller means generating a predetermined message signal in the form of digital speech samples for transmission on a predetermined one or more of said allocated channels to be received by said digital signal processing means which in response converts said speech signals into PCM speech signals and transmits said PCM speech signals to a predetermined one or more of said input/output ports via additional ones of said allocated channels.

14. A digital signal processing system as defined in claim 1, 2 or 3, wherein said digital signal processing means transmits successive interrupt signals to said main controller means for initiating transfer of successive message signals from said main controller means thereto via said digital switching

means, and said main controller means generates control signals to said digital signal processing thereby enabling further message signals to be transmitted.

15. A digital signal processing system as defined in claim 1, 2 or 3, wherein said digital switching means transmits an interrupt signal to said digital signal processing means along a dedicated message link for synchronizing PCM signal transmission along said allocated channels therebetween.

16. A digital signal processing system as defined in claim 1, said digital signal processing means being further comprised of first, second and third DSP modules for implementing first, second and third ones of said service features, respectively, said first service feature being multi-channel DTMF tone detection, said second feature being digital call conferencing, and said third feature being programmable tone generation and detection.

17. A digital signal processing system as defined in claim 16, wherein said first DSP module provides up to five PCM channels of simultaneous DTMF tone detection, said second module provides up to nineteen channels of digital call conferencing for supporting nine conference calls, and said third module provides a thirty-seven tone plant and two PCM channels of DFT tone detection.

18. A digital signal processing system as defined in claim 17, wherein three dedicated PCM links interconnect said digital switching means with said first, second and third DSP modules, odd channels being allocated to said first and second modules, and even channels of said three PCM links being allocated to said third modules.

19. A digital signal processing system as defined in claim 1, 2 or 3, wherein said digital switching means transmits a command byte to said digital signal processing means for enabling implementation of said one or more service features.

20. A digital signal processing system substantially as hereinbefore described with reference to and as illustrated by the accompanying diagrammatic drawings.

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